I. AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions of claims in the application.

1) (cancelled)

2) (Previously presented) A switch fabric as defined in claim 3, wherein the parameter is priority, the characteristic element being a priority level of a group of priority levels.

3) (currently amended) A switch fabric implemented on a chip comprising:
   a) an array of cells; and
   b) an I/O interface in communication with said array of cells permitting exchange of data packets between said array of cells and components external to said array of cells;
   c) each cell of said array including:
      I) a memory for holding a plurality of data packets for transmission to other cells of said array, each data packet of the plurality of data packets having a characteristic element represented by a parameter, the parameter allowing to distinguish one data packet from another data packet in the plurality of data packets;
      II) a control entity operative to:
         (i) select at least one data packet from the plurality of data packets at least in part on a basis of the parameter; and
         (ii) transmit the selected data packet to another cell of said array of cells;
      III) a transmitter in communication with said I/O interface and in communication with every other cell of said array, said transmitter

operative to process a data packet received from said I/O interface to determine a destination of the data packet and forward the data packet to at least one cell of said array selected on a basis of the determined destination;

IV) a set of receivers, wherein for each said other cell of said array, a respective receiver from said set of receivers is associated with said other cell, the respective receiver being in communication with said other cell allowing said other cell to forward data packets to the respective receiver; the receivers being in communication with said I/O interface for releasing data packets to said I/O interface.

4) (original) A switch fabric as defined in claim 3, wherein said array of cells includes a plurality of data channels, each data channel being associated with a given cell, the data channel associated with said given cell connecting the transmitter of said given cell to receivers in cells other than said given cell and associated with said given cell.

5) (previously presented) A switch fabric as defined in claim 2, wherein the data channel associated with said given cell connects the transmitter of said given cell to a receiver in every cell of said array of cells and associated with said given cell.

6) (original) A switch fabric as defined in claim 5, wherein the plurality of data channels are independent from one another, wherein transmission of a data packet over one data channel is made independently of a transmission of a data packet over another data channel.

7) (original) A switch fabric as defined in claim 6, wherein each data channel performs a parallel data transfer.

8) (original) A switch fabric as defined in claim 7, wherein said memory and said control entity form part of said transmitter.

9) (original) A switch fabric as defined in claim 8, wherein said memory includes a plurality of segments, each segment being associated with a receiver in a cell of said array to which the transmitter of said given cell is capable of forwarding a data packet via the data channel.

10)(original) A switch fabric as defined in claim 9, wherein said control entity is operative to process a data packet forwarded from said I/O interface to determine a cell of said array to which the data packet is destined and identify on a basis of the determined cell a segment of said memory into which the packet is to be loaded.

11)(original) A switch fabric as defined in claim 10, wherein said control entity includes a plurality of queue controllers associated with respective segments of said memory.

12)(original) A switch fabric as defined in claim 11, wherein said memory implements a plurality of registers, each register being associated with a queue controller and being suitable for holding data representative of a degree of occupancy of a segment of said memory associated with the queue controller.

13)(original) A switch fabric as defined in claim 12, wherein each segment of said memory is partitioned in slots, each slot capable of storing at least one data packet, each slot being associated with a given priority level of said group of priority levels.

14)(original) A switch fabric as defined in claim 13, wherein the registers of said memory associated with each queue controller store data indicative of a degree of occupancy of the slots of said segment associated with the queue controller, for each priority level of the group of priority levels.

15)(original) A switch fabric as defined in claim 14, wherein the transmitter of said given cell communicates with each receiver associated with said given cell to assess a degree of occupancy of each receiver associated with said given cell.

16)(original) A switch fabric as defined in claim 15, wherein the transmitter of said given cell communicates with each receiver associated with said given cell to assess the degree of occupancy of each receiver associated with said given cell over a back channel.

17)(original) A switch fabric as defined in claim 16, including a plurality of back channels, there being a dedicated back channel between the transmitter of said given cell and each receiver associated with said given cell.

18)(original) A switch fabric as defined in claim 17, wherein each back channel transfers data serially.

19)(original) A switch fabric as defined in claim 18, wherein said memory includes an area for storing data indicative of the degree of occupancy of each receiver associated with said given cell.

20)(original) A switch fabric as defined in claim 19, wherein said control entity is operative to process the data indicative of the degree of occupancy of each receiver associated with said given cell to determine which data packet stored in said memory is suitable for transmission to a receiver.

21)(original) A switch fabric as defined in claim 20, wherein said control entity determines that a data packet is suitable for transmission to a certain receiver when the data indicative of the degree of occupancy of the certain receiver indicates that the receiver is capable of accepting the data packet.

22)(original) A switch fabric as defined in claim 21, wherein when said control entity determines that a group of data packets are suitable for transmission, said control entity generates a plurality of control signals to request transmission of the data packets, each control signal being associated with a data packet.

23)(original) A switch fabric as defined in claim 22, wherein said control entity includes an arbiter for processing said control signals to select a data packet to transmit among the group of data packets suitable for transmission.

24)(original) A switch fabric as defined in claim 23, wherein each control signal conveys the priority level of the data packet associated with the control signal.

25)(original) A switch fabric as defined in claim 24, wherein said arbiter selects a data packet to transmit among the group of data packets suitable for transmission on a basis of the priority levels of the group of data packets suitable for transmission.

26)(original) A switch fabric as defined in claim 25 wherein said arbiter processes control signals to request transmission of data packets in a round robin manner.

27)(original) A switch fabric as defined in claim 26, wherein said arbiter selects a data packet to transmit among the group of data packets suitable for transmission on a basis of the priority levels of the packets in the group of data packets suitable for transmission and on the basis of whether or not a data packet was previously submitted for transmission.

28)(original) A switch fabric as defined in claim 6, wherein said memory is a first memory, said switch fabric including a second memory wherein said second memory includes a plurality of sectors associated with respective receivers of said plurality of receivers, said sectors capable of storing data packets forwarded to said receivers by cells of said array.

29)(original) A switch fabric as defined in claim 28, wherein each receiver of said plurality of receivers communicates with said I/O interface.

30)(original) A switch fabric as defined in claim 29, wherein said control entity is a first control entity, said switch fabric including a second control entity to regulate a release of data packets from said sectors to said I/O interface.

31)(original) A switch fabric as defined in claim 30, wherein said second control entity includes a plurality of queue controllers associated with respective sectors of said second memory.

32)(original) A switch fabric as defined in claim 31, wherein a data packet received by a receiver of said plurality of receivers is characterized by a priority level selected in a group of priority levels, each sector of said second memory being divided in subdivisions each subdivision capable of storing at least one data packet, each subdivision being associated with a given priority level of said group of priority levels.

33)(original) A switch fabric as defined in claim 32, wherein said second control entity includes an arbiter in communication with said queue controllers, each queue controller operative to transmit a control signal to the arbiter of said second control entity for each data packet held in the sector associated with the queue controller to request release of the data packet to said I/O interface.

34)(original) A switch fabric as defined in claim 33, wherein each control signal conveys the priority level of the data packet associated with the control signal.

35)(original) A switch fabric as defined in claim 34, wherein said arbiter selects a data packet for release to said I/O interface among the data packets corresponding to the control signals transmitted to the arbiter of said second control entity on the basis of the levels of priority of the data packets corresponding to the control signals.

36)(previously presented) A switch fabric as defined in claim 3, wherein said control entity is operative to alter the parameters associated with respective data packets of the plurality of data packets.

37)(original) A switch fabric as defined in claim 2, wherein said control entity is operative to alter the priority levels associated with respective data packets of said plurality of data packets.

38)(original) A switch fabric as defined in claim 37, wherein said control entity is operative to alter the priority level associated with a given data packet of said plurality of data packets at least in part on a basis of a time of residence of the given data packet in said memory.

39)(original) A switch fabric as defined in claim 38, wherein said control entity is operative to alter the priority level associated with the given data packet according to a function that relates the priority level of the given data packet to the time of residence of the data packet, the function selected in the group consisting of linear function, exponential function and logarithmic function.

40)(original) A switch fabric as defined in claim 3, wherein each data packet comprises a plurality of words including a first word of said data packet and a last word of said data packet, wherein each word comprises a field indicative of whether said word is a pre-determined number of words away from said last word of said data packet.

41)(original) A switch fabric as defined in claim 40, wherein the transmitter is operative to monitor said field in each word of each data packet forwarded to at least one cell of said array, the transmitter further being operative to begin forwarding a next data packet upon detecting that said field of a word in a packet currently being forwarded is indicative of said word being a pre-determined number of words away from the last word of said data packet currently being forwarded.

42)(original) A switch fabric as defined in claim 3, each cell further including a central processing unit (CPU) connected to the transmitter, said transmitter being further operative to process a data packet received from said CPU to determine a destination of the data packet and forward the data packet to at least one cell of said array selected on the basis of the determined destination.

43)(original) A switch fabric as defined in claim 4, each cell further including a central processing unit (CPU) connected to the transmitter, said transmitter being further operative to process a data packet received from said CPU to

determine a destination of the data packet and forward the data packet to at least one cell of said array selected on the basis of the determined destination, wherein data packets received by the transmitter in a given cell from the I/O interface and from the CPU in said given cell share the data channel associated with said given cell.

44)(original) A switch fabric as defined in claim 3, each cell further including a central processing unit (CPU) connected to the plurality of receivers, said receivers being further operative to determine whether data packets are to be released to the I/O interface or to the CPU and release said data packets accordingly.

45)(original) A switch fabric as claimed in claim 44, wherein each data packet comprises a field indicative of whether the data packet is destined for a CPU and wherein said receivers are operative to determine whether data packets are to be released to the I/O interface or to the CPU on the basis of said field.

46)(original) A switch fabric as defined in claim 22, each cell further including a central processing unit (CPU) connected to the plurality of receivers, wherein said control entity includes a first arbiter for processing said control signals to select a data packet to transmit to the I/O interface among the plurality of data packets suitable for transmission to the I/O interface, wherein said control entity includes a second arbiter for processing said control signals to select a data packet to transmit to the CPU among the plurality of data packets suitable for transmission to the CPU.